ABSTRACT OF THE INVENTION

A three step process for planarizing an integrated circuit structure comprising one or more dielectric layers having trench and/or via openings therein lined with a layer of electrically conductive barrier liner material and filled with copper filler material.

Sufficient excess copper (formed over the barrier liner portions on the top surface of the dielectric layer) is removed in an initial chemical mechanical polish (CMP) step to provide a planarized copper layer with a global planarity of about 20 nm to about 30 nm. The remainder of the excess copper over the portion of the barrier liner material lying on the top surface of the dielectric layer is then removed by electropolishing the structure, in a second step, until all of the excess copper over the portion of the barrier liner material lying on the top surface of the dielectric layer is removed. In a third step, all remaining portions of the diffusion barrier liner on the upper surface of the low k dielectric layer are then removed using a dry etching process selective to copper and the dielectric layer until all of the portions of the barrier layer over the top surface of the dielectric layer are removed; whereby the integrated circuit structure may be planarized by removal of all of the copper layer and barrier layer from the top surface of the dielectric layer while inhibiting dishing and/or erosion of the surface of copper filler material in the opening, and without risking distortion and/or delamination by the harsh effects of excessive CMP processing.